1.   A method of performing additive synthesis of digital audio signals in a recursive digital oscillator, comprising:
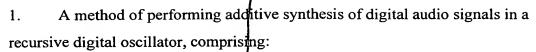
5   receiving digital audio signal frames wherein each digital audio signal frame includes a set of frequency, amplitude, and phase components represented as coefficients of variables in a mathematical expression, each digital audio signal frame thereby including a frequency coefficient representation;

          forming converted frequency coefficients by linearaly re-mapping of bits of
10   said frequency coefficient representation to bias audio reproduction accuracy toward low frequency signals; and

          performing additive synthesis with said converted frequency coefficients.

2.   The method of claim 1 further comprising the step of defining said frequency
15   coefficient representation with an exponent characterizing a floating-point range extension.

3.   The method of claim 2 wherein said defining step includes the step of specifying said exponent to correspond to a right shift amount necessary to correct for
20   precision limitations introduced by limiting re-mapping coefficients to 16 bits.

4.   The method of claim 3 wherein said receiving, forming, and performing steps are implemented utilizing a 16-bit fixed point processor.

25   5.   The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a digital signal processor.

6.   The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a field programmable gate array.

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7.   The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a Very Long Instruction Word processor.

8.   The me●of claim 1 wherein said receiving, for●, and performing steps are implemented utilizing a Reduced Instruction Set Computer.

9.   The method of claim 1 wherein said receiving, forming, and performing steps
5   are implemented utilizing a Residue Number System processor.

10.   A computer readable memory to direct a processor to function in a specified manner, comprising:
        a first set of executable instructions to receive digital audio signal frames
10   wherein each digital audio signal frame has a set of specified frequency values expressed as a bit sequence;
        a second set of executable instructions to transform said bit sequence to represent lower frequencies with more significant bits and higher frequencies with less significant bits; and
15   a third set of executable instructions to facilitate additive synthesis of said digital audio signal frames in a reduced-precision recursive digital oscillator.

11.   The computer readable memory of claim 10 wherein said first set of executable instructions include instructions to identify a frequency coefficient representation of
20   said specified frequency.

12.   The computer readable memory of claim 11 further comprising a fourth set of executable instructions to define said frequency coefficient representation with an exponent characterizing a floating-point range extension.

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13.   The computer readable memory of claim 12 wherein said fourth set of executable instructions include instructions to specify said exponent to correspond to a right shift amount necessary to correct for precision limitations introduced by a reduce precision processor.